AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): An apparatus for detecting an operation value for input data comprising:

a means for storing seed values corresponding to seed points determined according to a range of the input data and output data and an error rate;

an address and data generator for comparing a predetermined reference value with the input data to generate an address of the storing means and revised input data corresponding to the input data; and

an operator for performing a predetermined operation to output an operation value corresponding to the input data, using the seed values output from the storing means and the revised input data generated by the address and data generator.

2. (original): The apparatus of claim 1, wherein the seed values stored in the storing means consist of values corresponding to unevenly spaced seed points.

3. (original): The apparatus of claim 2, wherein the unevenly spaced seed points are formed by adding a new seed point between evenly spaced seed points until an error value satisfies error rate conditions available from an operation value detecting apparatus, wherein the error value is detected using a real operation value for an arbitrary point between the evenly spaced seed points determined by the input data bits and an operation value using the evenly spaced seed points and seed values corresponding to the seed points.

4. (original): The apparatus of claim 2, wherein the address and data generator comprises:

a comparison unit for comparing the predetermined reference values with the input data;

an index generator for generating predetermined index information according to a comparison result output from the comparison unit;

an address generator for generating addresses corresponding to the input data based on the index information output from the index generator; and

a revised input data generator for generating revised input data corresponding to the input data based on the index information output from the index generator.

5. (currently amended): The apparatus of claim 4, wherein the predetermined reference values are set before values corresponding to ~~depending on exponents~~ powers of 2, which correspond~~ing~~ to the differences between real seed addresses, ~~which correspond to the seed values stored in the storing means~~are changed.

6. (currently amended): The apparatus of claim 5, wherein the comparison unit consists of comparators for setting the predetermined reference values as the real seed addresses before the ~~exponent~~ power of 2 corresponding to the difference in addresses is changed.

7. (currently amended): The apparatus of claim 6, wherein the number of the comparators is equal to the number of ~~exponents~~ powers of 2 having different values when the value representing the power of 2 is used for seeds stored in the storing means.

8. (currently amended): The apparatus of claim 4, wherein the index generator analyzes the comparison result and outputs a~~n~~ value corresponding to a ~~exponent~~ power of 2,

said power of 2 corresponding to ~~the~~ a difference between ~~the~~ real seed addresses, ~~corresponding to the input data~~ as the index information.

9. (original): The apparatus of claim 4, wherein the address generator generates corresponding upper and lower addresses depending on the result of determining which of the real seed addresses of the storing means approaches the input data based on the index information.

10. (original): The apparatus of claim 9, wherein the operator multiplies the difference between a first seed value stored in the storing means corresponding to the upper address and a second seed value stored in the storing means corresponding to the lower address by the revised input data, divides the multiplied result by the difference between the upper address and the lower address, subtracts the divided result from the first seed value, and outputs the subtracted result as an operation value corresponding to the input data.

11. (original): The apparatus of claim 4, wherein the revised input data generator determines bits to be output on the basis of the least significant bit of the input data, and outputs the determined bits as the revised input data.

12. (original): The apparatus of claim 1, wherein the address and data generator comprises:

a comparison unit for comparing the predetermined reference values with the input data;

an index generator for generating predetermined index information depending on a comparison result output from the comparison unit;

an address generator for generating addresses corresponding to the input data based on the index information output from the index generator; and

a revised input data generator for generating revised input data corresponding to the input data based on the index information output from the index generator.

13. (original): The apparatus of claim 1, wherein the storing means consist of a look-up table.

14. (currently amended): A method for detecting an operation value corresponding to input data comprising the steps of:

(a) storing seed values corresponding to seed points determined according to ranges of the input data and output data and an error rate;

(b) analyzing which addresses of the stored seed values approach the input data;

(c) generating an upper address and a lower address corresponding to the input data according to the analyzed result in the step (b);

(d) reading seed values corresponding to the upper and lower addresses generated in the step (c) from the seed values stored in the step (a);

(e) revising the input data according to the analyzed result in the step (b); and

(f) performing a predetermined operation using ~~the upper and lower addresses,~~ the seed values read in the step (d), and the revised input data, to output an operation value corresponding to the input data.

15. (original): The method of claim 14, wherein the step (a) comprises the steps of:

(a1) determining input and output data bits depending on the ranges of the input data and output data;

(a2) determining seed points in an evenly spaced manner depending on the determined input data bits;

(a3) comparing the difference between a real operation value for an arbitrary point between first and second seed points determined in the step (a2) and an operation value using seed values corresponding to the first and second seed points with a predetermined reference value;

(a4) setting the first and second seed points as seed points if the difference between the operation values is less than the predetermined reference value; and

(a5) adding the arbitrary point as the seed point existing between the first and second seed points if the difference between the operation values is not less than the first predetermined reference value.

16. (original): The method of claim 15, further comprising the step of repeatedly performing the steps (a3) through (a5) until the difference between the operation values is less than the predetermined reference value.

17. (currently amended): The method of claim 14, wherein the step (b) comprises the steps of:

(b1) setting a real seed address as a reference value before ~~the~~a value that corresponds to a ~~exponent~~ power of 2, said power of 2 corresponding to the difference between real seed addresses for the seed values, is changed; and

(b2) comparing the reference value with the input data to output the result of analyzing which of the real seed address approaches the input data.

18. (original): The method of claim 14, wherein the step (e) comprises the steps of:

(e1) determining bits to be output based on the least significant bit of the input data; and

(e2) outputting the determined bits along with the input data as revised input data.